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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,355	10/31/2003	Peter J. Zievers	ZIEVERS 3	5404

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EXAMINER	
KRAVETS, LEONID	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 12/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,355	ZIEVERS, PETER J.	
	Examiner	Art Unit	
	Leonid Kravets	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters 802, 803, 804 and 902,903, 904 have both been used to designate the same parts in different drawings. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 200, 400, 500, 501, 502, 503, 504, 506, 507, 508, 800 etc. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any

amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 3 recites the limitation "processes" this should be "process". Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed.

Cir. 1999). The term "write request" in claim 2 is used by the claim to mean "read", while the accepted meaning is "write." The term is indefinite because the specification does not clearly redefine the term. A write request is not necessary to read a data file. Examiner interprets the write request to be a read request.

6. The term "read request" in claim 17 is used by the claim to mean "write", while the accepted meaning is "read." The term is indefinite because the specification does not clearly redefine the term. A read request is not necessary to write a data file. Examiner interprets the write request to be a read request.

7. Claim 10 recites the limitation "the multiple file requests". There is lack of antecedent basis for this limitation. Examiner interprets this as "a file request".

8. Claims 16 and 18 recite the limitation "the busy/idle state". There is insufficient antecedent basis for this limitation in the claim. Examiner interprets this to be a selector signal.

Double Patenting

9. Copending applications 10/699,355 (instant) and 10/699,315 were found to have obviousness-type provisional double-patenting issues.

10. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory

obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

11. Claims 1-4 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-4 of copending Application No. 10/699,315. Claims 1-4 of the instant application are anticipated by claims 1-4 of the referenced application in that the claims contain all the limitations of the instant claims. The claims are not patentably distinct from each other because the instant application claims a data file having a first portion and an excess portion. The referenced application defines a linked list having a first portion (head buffer) and an excess portion (intermediate buffers).

This is a provisional obviousness-type double patenting rejection based on anticipation analysis because the conflicting claims have not in fact been patented.

With respect to claim 1 of the instant application, please refer to the table below, which illustrates the anticipator relationship of the claims at issue:

Instant Application 10/699355	Application 10/699315
1. A method of operating a memory management system adapted to process data files	1. A method of operating a memory management system for processing linked list data files
An access flow regulator	An access flow regulator
A plurality of high speed low storage capacity memories	A plurality of low storage capacity high speed memories
A lower speed high storage capacity bulk memory	A lower speed high storage capacity bulk memory
High speed memories have a first data rate	High speed memories have a first data rate
Bulk memory has a second data rate substantially lower than said first data rate	Bulk memory has a second data rate lower than said first data rate
Operating said access flow regulator for generating requests for the reading and writing of said memories	Access flow regulator for generating requests for the reading and writing of linked lists by said memories [Memories consist of linked lists, thus access flow regulator writes the memories]
Initiating the writing of a data file by transmitting a write request from said access flow regulator to one of said high speed memories	Initiating the writing of a linked list in said high speed memories by transmitting a write request from said access flow regulator to said high speed memories [a linked-list is a type of data file]
Data file has a first portion and an excess portion	[Linked list consists of several buffers, thus there is inherently a first portion and an excess portion]
Writing said first part and said excess portion of said data file into said one high speed memory	Writing a head buffer and a tail buffer and at least one intermediate buffer of said linked list into said high speed memories [Head buffer is the first part. Intermediate buffer is the excess part]
Transferring said excess portion of said data file from said one high speed memory to said bulk memory while leaving said first portion of said data file in said one high speed memory.	Transferring said at least one intermediate buffer from said high speed memories to said bulk memory while leaving the head buffer and the tail buffer in said high speed memories.

Claim 2 of the instant application is provisionally rejected on the ground of nonstatutory obviousness-type double patenting on claim 2 of the referenced application.

Claim 3 of the instant application is provisionally rejected on the ground of nonstatutory obviousness-type double patenting on claim 3 of the referenced application.

Claim 4 of the instant application is provisionally rejected on the ground of nonstatutory obviousness-type double patenting on claim 4 of the referenced application.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

13. Claims 1-4 and 17 rejected under 35 U.S.C. 102(e) as being anticipated by Ferguson.

14. As per claim 1, Ferguson discloses a method of operating a memory management system for processing data files (Col 41, Lines 43-48), said system

comprising an access flow regulator (Col 41, Lines 31-35), a plurality of high speed low storage capacity memories [Ferguson describes queues implemented on a per-port basis, thus each port has its own queue and memory (Col 41, Lines 42-46)] and a lower speed high storage capacity bulk memory (Fig 3, Ref 319), said high speed memories have a first data rate, said bulk memory has a second data rate substantially lower than said first data rate, said method comprises the steps of:

operating said access flow regulator for generating requests for the reading and writing of said memories (Col 41, Lines 31-35);

initiating the writing of a data file by transmitting a write request from said access flow regulator to one of said high speed memories, said data file has a first portion and an excess portion [Note data file is the cells as a linked-list in the case of Ferguson (Col 41, Lines 31-35)];

writing said first part and said excess portion of said data file into said one high speed memory (Col 41, Lines 31-35); and

transferring said excess portion of said data file from said one high speed memory to said bulk memory while leaving said first portion of said data file in said one high speed memory (Col 41, Lines 57-60).

15. As per claim 2, Ferguson discloses a method of operating a memory management system for processing data files (Col 41, Lines 43-48), said system comprising an access flow regulator (Col 41, Lines 31-35), a plurality of high speed low storage capacity memories [Ferguson describes queues implemented on a per-port

basis, thus each port has its own queue and memory (Col 41, Lines 42-46)] and a lower speed high storage capacity bulk memory (Fig 3, Ref 319), said high speed memories have a first data rate, said bulk memory has a second data rate substantially lower than said first data rate, said method comprises the steps of:

operating said access flow regulator for generating requests for the reading and writing of said memories (Col 41, Lines 31-35);

initiating the reading of a data file by transmitting a write request from said access flow regulator to one of said high speed memories, said data file has a first portion and an excess portion (Col 43, Lines 20-21);

transmitting a read request for a data file from said access flow regulator to a one high speed memory storing a first part of said data file (Col 43, Lines 28-30);

reading said first portion of said data file from said one high speed memory (Col 43, Lines 20-21);

transferring said excess portion of said data file from said bulk memory to said one high speed memory [it is inherent that once a head buffer is read, a new buffer will replace it given that the head buffer is the top of the queue];

reading out said excess portion of said data file from said one high speed memory [The intermediate buffer is now the head buffer, thus the method repeats (Col 43, Lines 20-21)]; and

transmitting said first part and said excess portion said data file to said access flow regulator [Buffer of Ferguson is within the multi-function multi-port along with the

output request processor making the read requests, thus they are one unit (Col 44, Lines 8-10)].

16. As per claim 3, Ferguson discloses the method of claim 1 further including the step of operating said system to concurrently processes data files for a plurality of requests from said access flow regulator [Output switch communicates directly with each output request processor, thus these units are considered one access flow regulator. The output switch transmits to the output request processors of each multi-function multiport (Col 41, Lines 9-11)].

17. As per claim 4, Ferguson discloses the method of claim 1 further including the step of operating said system to concurrently process a plurality of data files stored in different ones of said high speed memories [the linked list queues in each multi-function multiport are independent and thus are processed in different high speed memories (Col 41, Lines 20-26)].

18. As per claim 17, please see rejections of claims 1 and 2 above. Claim 17 is a combination of these two claims.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

21. Claims 5-6, 13, 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ferguson as applied to claim 1 above, and further in view of Brigati (US Patent 6,279,068).

As per claim 5, Ferguson discloses the method of claim 1 wherein said system further comprises a plurality of state controllers each of which is individual to one of said high speed memories (Fig 3, Ref 306), said system further comprises an access bus connecting said access flow regulator with said state controllers (Fig 3, Ref 102). Ferguson does not disclose the method wherein said step of transmitting a read request includes the steps of:

operating said access flow regulator to select an idle high speed memory that is to receive said write request;

transmitting said write request from said access flow regulator over said request bus to the state controller individual to said selected high speed memory; and

operating said state controller to extend said write request to the high speed memory.

Brigati and Ferguson further disclose the method wherein said step of transmitting a read request includes the steps of:

operating said access flow regulator to select an idle high speed memory that is to receive said write request (Brigati, Col 2, Lines 24-27; Col 3, Lines 4-8);

transmitting said write request from said access flow regulator over said request bus to the state controller individual to said selected high speed memory [The access flow regulator must transmit to the state controller individual to said selected high speed memory, as in the system of Ferguson only output switch 102 connects each multi-function multiport to the output switch (Fig 3, Ref 102)]; and

Ferguson further discloses operating said state controller to extend said write request to the high speed memory (Col 41, Lines 31-35).

As per claim 6, Ferguson and Brigati disclose the method of claim 5 wherein said step of operating said state controller to transmit said write request includes the steps of:

determining the present occupancy level of said selected high speed memory (Ferguson, Col 42, Lines 22-24);

transmitting said request to said selected high speed memory if said present occupancy is not exceeded (Ferguson, Col 42, Lines 19-22); and

requesting a signalwise connection of said access flow regulator to said

bulk memory if said present occupancy level of said selected high speed memory is exceeded [Since when the occupancy level is exceeded, most cells are stored in bulk memory, a connection to bulk memory must be made to read data that has been moved into this memory from the high speed queue (Ferguson, Col 42, Lines 22-24)].

As per claim 13, Ferguson and Brigati disclose the method of claim 5 wherein said step of operating said state controllers includes the further steps of:

determining whether said bulk memory is idle when a transfer is requested;

extending said data file to said bulk memory if said bulk memory idle; and

buffering said transfer request if said bulk memory is busy.

[It would have been obvious to one of ordinary skill in the art to transfer a buffer to bulk memory if the bulk memory is idle or to buffer the transfer if it is busy for later transfer].

As per claim 16, Ferguson discloses the method of claim 1. Brigati discloses the method comprising the further steps of:

generating a signal unique to each said high speed memory indicating the busy/idle state of each said high speed memory (Paragraph 17);

extending each generated signal to said access flow regulator [The signal must be extended to the access flow regulator for it to be able to make decisions on where to send the data];

operating said access flow regulator to receive requests for the writing or reading of files by said memories (Ferguson, Col 41, Lines 9-11) ;

operating said access flow regulator in response to the receipt of said request to read said busy/idle signals [Brigati discloses using the selection signal to select an idle memory, in the system of Ferguson, this task would be performed by the output processor (Brigati, Paragraph 17)];

operating said access flow regulator in response to said reading to identify an idle one of said memories [In the system of Brigati, the idle memory is the one which is not being written and thus can be selected from the selection signals (Brigati, Paragraph 17)]; and

operating said access flow regulator for extending a request for the reading and writing of a data file to said idle one high speed memory [Brigati discloses extending a read/write request to the idle memory (Paragraph 11)].

As per claim 18, please see rejection of claims 16 and 17. Claim 18 is a combination of these two claims.

With regard to claims 5-6, 13, 16 and 18, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the selection of idle memory of Brigati into the system of Ferguson, since Ferguson and Brigati form the same field of endeavor, namely data transfer between memories and this would allow for reads and writes to not have to wait for a busy memory to become idle (Brigati, Paragraph 11).

22. Claims 9 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ferguson as applied to claim 2 above, and further in view of Milway (US Patent 6,470,428).

As per claim 9, Ferguson discloses the method of claim 2.

Ferguson and Milway further disclose the method wherein said step of transferring said data file from said bulk memory includes the steps of:

reading out files from said bulk memory to said high speed memories in a burst mode at a data rate substantially equal to the data rate of said high speed memories (Milway, Col 1, Lines 59-64);

storing said read out files in said high speed memories (Ferguson, Col 42, Lines 9-11); and

reading out said data file from said high speed memory for transfer to said access flow regulator [Buffer of Ferguson is within the multi-function multi-port along with the output request processor making the read requests, thus they are one unit (Ferguson, Col 44, Lines 8-10)].

As per claim 12, Ferguson and Milway disclose the method of claim 5 wherein said step of operating said state controllers includes the further steps of:

controlling the transfer of a data file from said high speed memory to said bulk memory [Milway discloses using burst transfers, while Ferguson discloses transferring cells from the head-tail buffer to the notification area (Milway Col 1, Lines 59-64;

Ferguson Col 42, Lines 22-24). While the system of Milway transfers data in bursts from memory to cache, a person of ordinary skill in the art would understand that the opposite transfer would serve the same purpose of speeding up memory transfers]; and

controlling the transfer of a data file from said bulk memory to said high speed memories (Ferguson, Col 42, Lines 6-11).

With regard to claims 9 and 12, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the burst transfer of Milway into the system of Ferguson, since Ferguson and Milway form the same field of endeavor, namely multi tiered memory hierarchies and this would allow for faster transfer of data between the storage and memory by transferring several data units at once (Milway, Col 1, Lines 61 63).

23. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ferguson in view of Brigati as applied to claim 5 above, and further in view of Klikki (US Patent 6,868,061.

As per claim 11, Ferguson and Brigati disclose the method of claim 5, wherein said step of operating said state controller includes the further steps of:

processing each received request to determine the present occupancy level of said high speed memory (Col 6, Lines 51-54);

extending said request to said high speed memories if said present occupancy level is not exceeded (Col 7, Lines 49-53); and

buffering said request in said access flow regulator if said present occupancy level is exceeded [The system of Klikki discards cells once the occupancy level threshold is exceeded, however, one of ordinary skill in the art would understand that instituting a buffer for these cells would allow for less dropped packets and thus better network reliability (Col 7, Lines 45-49)].

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the occupancy level of Klikki into the system of Ferguson and Brigati, since Ferguson, Brigati and Klikki form the same field of endeavor, namely packet routing and this would allow for more even usage of memory buffers.

24. Claims 7-8 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ferguson in view of Brigati as applied to claim 5 above, and further in view of Lee et al. (US PG Pub 2004/0205305).

As per claim 7, Ferguson and Brigati disclose the method of claim 5. They do not disclose the method wherein said system further includes a multiplexer, and an access bus connecting said state controllers with said multiplexer.

Lee discloses such a multiplexer (Fig 1, Ref 54), and an access bus connecting memories to a multiplexer (Fig 1, Ref 50). The system of Lee further includes a bus connecting said multiplexer with said bulk memory; said method includes the further steps of:

transmitting a request to said multiplexer for the transfer of data files from said state controllers to said bulk memory [In the system of Lee, FIFOs request transfer of data files to a bulk memory (Fig 1). The system of Ferguson and Brigati would use such a multiplexer to create one bulk memory for all the multi-function multiports and to transfer cells from the head-tail queues to a common notification memory];

determining which one of a plurality of requesting state controllers is to be granted access to said bulk memory [A multiplexer selects one input from several possible inputs to output (Fig 1, Ref 54)];

connecting signalwise said one requesting state controller to said bulk memory [A multiplexer selects one input from several possible inputs to output, thus connecting the FIFO of Lee to the memory]; and

controlling the operation of said bulk memory in the transfer of data from said selected high speed memory to said bulk memory [Multiplexer can connect or disconnect any memory, thus it controls the operation of the bulk memory in the transfer of data].

As per claim 8, Ferguson Brigati and Lee disclose the method of claim 7 including the further step of applying said data file from said high speed memory and

said state controller via said multiplexer and said bus to said bulk memory [The system of Ferguson and Brigati transfers cells from the head-tail queue to the memory. In the system of Ferguson, Brigati and Lee, .the addition of a multiplexer allows to apply the data file from head-tail queue to a central bulk memory (Lee, Fig 1; Ferguson, Col 42, Lines 22-24)].

As per claim 14, Ferguson discloses the method of claim 7 wherein said step of operating said multiplexer includes the further steps of:

determining which one of a plurality of requesting high speed memories is to be granted access to said bulk memory [A multiplexer selects one input from several possible inputs to output (Fig 1, Ref 54)];

granting the request to one of said high speed memories [Granting the request is interpreted as connecting the high-speed memory to the bulk memory, an operation the multiplexer is meant to perform]; and

buffering the requests of all but said one high speed memories [Though Lee does not expressly disclose a buffer in the multiplexer, one of ordinary skill in the art would have found it obvious to add such a buffer to the multiplexer in order to free the high speed memories from waiting to transfer to the bulk memory, thus allowing them to perform other such as storing new cells in the head-tail queue of Ferguson].

As per claim 15, Ferguson discloses the method of claim 7 wherein said step of operating said multiplexer includes the further steps of:

determining the identity to the one of said high speed memories to which a data file is to be directed by said multiplexer [A multiplexer must select one of the possible outputs to transfer to, thus it identifies an output]; and

controlling the transfer of said data file from said bulk memory to said identified high speed memory [The task of a multiplexer is to connect an input to an output, thus the multiplexer controls the transfer by connecting or disconnecting the input and the output]

With regard to claims 7-8 and 14-15, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the multiplexer of Lee into the system of Ferguson and Brigati, since Ferguson, Brigati and Lee form the same field of endeavor, namely data transfer between memories and this would allow for sharing of a bulk memory between the high-speed memory, providing a cost savings in the system.

Conclusion

1. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent 6,711,170 discloses a technique of bank balancing to provide for same level of occupancy among banks.

US Patent 6,842,826 discloses maintaining data blocks in a queue having a tail and a head end.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Kravets whose telephone number is 571-272-2706. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached at 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LK

Leonid Kravets
Patent Examiner
Art Unit 2189

November 22, 2005

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 21[illegible]